ELEC50001 – Circuits and Systems

2020 - 2021

Answer ALL questions.

There are THREE questions on the paper.

Question ONE counts for 50% of the marks, other questions 25% each

Time allowed: 2 hours

Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X[2:0] denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.

1. (a) Part of the datasheet for MCP601, an operational amplifier, is included at the end of this paper as Appendix A, and is also provided as a separate file for your convenience.

Based on the information available, answer the following questions with appropriate justifications.

(i) *Figure 1.1(a)* shows the MCP601 connected as unity gain buffer. Sketch the output signal V_{OUT} if the input signal V_{IN} is a symmetrical digital clock signal at a frequency of 100kHz with low and high logic levels at 0V and 3.3V.

[4]

(ii) What is the amplitude of V_{OUT} if V_{IN} varies between 1.1V and 1.2V and is a 2.8MHz sinusoidal signal with a DC offset?

[3]

(iii) *Figure 1.1(b)* shows a non-inverting audio amplifier circuit using MCP601. Choose the values of the resistors R1 to R4, C1 and C2 such that the amplifier provides a gain of 10 for signals in frequency range from 10Hz to 20kHz. Explain the reasons for your choices.

[5]

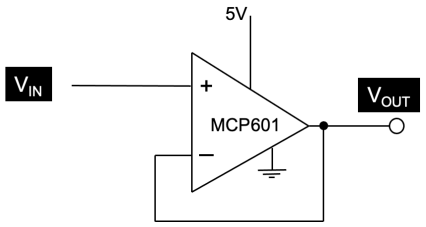

Figure 1.1(a)

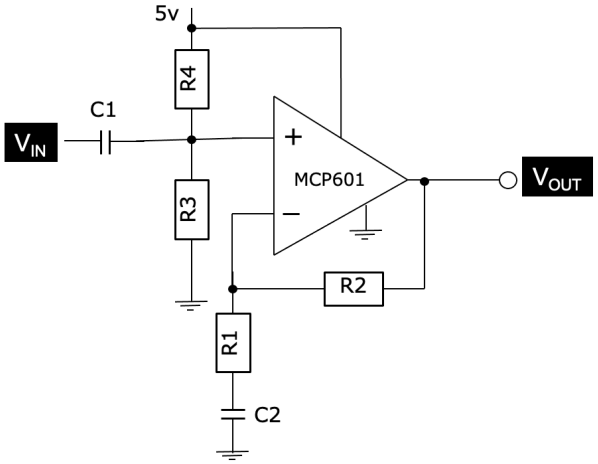

Figure 1.1(b)

(b) Internet Protocol (IP) address version 4 (IPv4) is specified as a 32-bit number divided into four 8-bit sub-addresses as shown in *Figure 1.2*. The address range 192.168.0.0 to 192.171.255.255 is to be reserved for private use.

(i) If the IP address is available as a digital signal IP[31:0], design in the form of a Boolean equation a decoder circuit that produces high active output signal Y whenever the IP address falls within the address range above.

[4]

(ii) Implement this decoder design in synthesizable Verilog HDL.

[4]

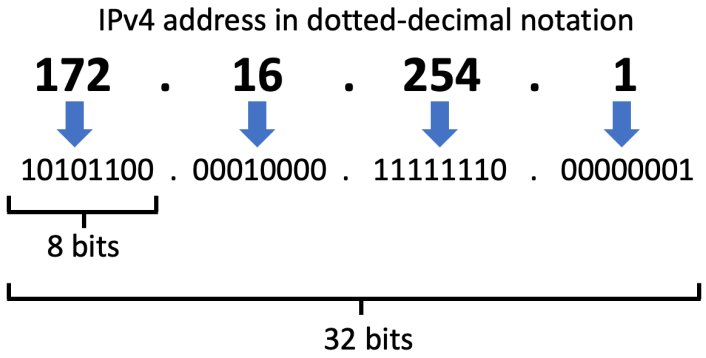

Figure 1.2

(c) *Figure 1.3* shows the interface definition for an up-down counter *updn* where the counter output *value* is incremented by one every time a rising edge is detected on *tick* if *up* is high, and is decremented by one if *up* is low. The output *value* is limited to a range between 0 and 100 and does not wrap around when these limits are reached.

Design the *updn* module in Verilog HDL.

[8]

```
1  module updn (tick, up, value);
2
3     input          tick;       // clock signalinput
4     input          up;         // high to count up
5     output [6:0]   value;
```

Figure 1.3

(d) In the circuit shown in *Figure 1.4*, A and B are combinational logic blocks with propagation delays t_{d_A} and t_{d_B} respectively, where 0.4ns < t_{d_A} < 0.8ns and 0.2ns < t_{d_B} < 0.4ns.

Flip-flops FF1 and FF2, both clocked by a symmetrical clock signal CLK, have a clock to Q delay t_{cq} of 0.5ns, setup-time t_s of 0.5ns, and a hold-time t_h of 0.9ns.

(i) By considering only the setup-time constraints, calculate the maximum operating frequency of the clock signal CLK for reliable operation of this circuit.

[4]

(ii) Show that there is hold-time violation for FF2 but not for FF1.

[4]

(iii) FF2 is replaced with a negative edge trigger flip-flop, and all timing constraints remain as before. Calculate the new maximum operating frequency of CLK and show that there is no longer a hold-time violation for FF1 and FF2.

[4]

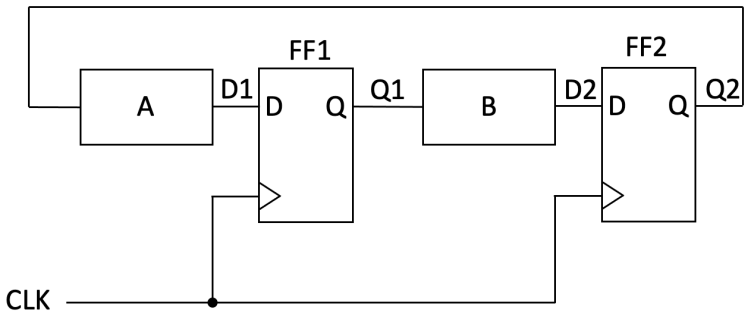

Figure 1.4

(e) *Figure 1.5(a)* shows the Verilog implementation of a module *digital_block* with a clock input *clk,* a 10-bit input *n[9:0]* and an output *out*.

(i) Sketch a block diagram showing the function of *digital_block*.

[5]

(ii) This circuit is driven by a 50MHz clock signal and an input N as shown in *Figure 1.5(b)*. Sketch the output signal Y. State any assumption used.

[5]

```
1   module digital_block(clk, n, out);
2
3      input          clk;        // clock signal
4      input [9:0]    n;
5      output         out;
6
7      reg [9:0]      v;
8      reg [5:0]      cnt;
9      reg            out, tick;
10
11     initial v = 10'b0;
12     initial cnt = 6'd49;
13
14     always @ (posedge clk)
15        if (cnt == 6'd0) begin
16           cnt <= 6'd49;
17           tick <= 1'b1;
18           end
19        else begin
20           cnt <= cnt - 1'b1;
21           tick <= 1'b0;
22           end
23
24     always @ (posedge tick) begin
25        if (v < 10'd999)
26           v <= v + 1'b1;
27        else
28           v <= 10'd0;
29        out <= (v < n);
30     end
31
32  endmodule
```

Figure 1.5(a)

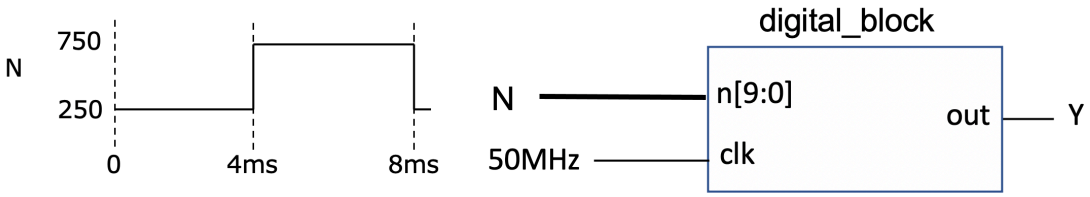

Figure 1.5(b)

2. *Figure 2.1* shows the state diagram of a Finite State Machine (FSM) with four states encoded using two state bits S1 and S0, an input P and an output Q.

(a) Draw the state transition table including the output for this state machine.

[5]

(b) The FSM is to be implemented using an Intel MAX10 FPGA using three Logic Elements LE0, LE1 and LE2. Each Logic Element consists of a 4-input lookup table (LUT) and an optional D-type flip-flop. *Figure 2.2* shows the circuit for the state transition logic of the FSM with LE0 and LE1. Derive the truth-tables for LUT0 and LUT1.

[7]

(c) Draw the circuit of LE2 which provides the output Q and derive the truth-table for LUT2.

[5]

(d) Write in Verilog HDL an implementation of this FSM using one-hot encoding.

[8]

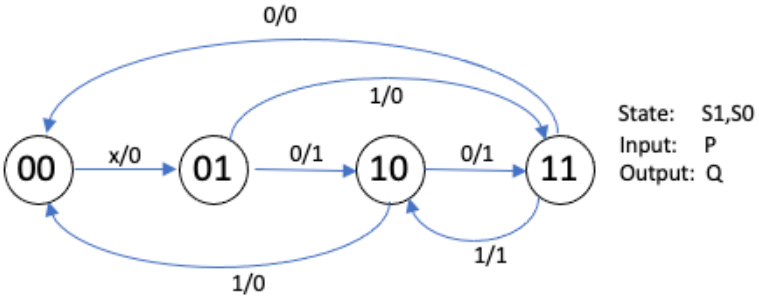

Figure 2.1

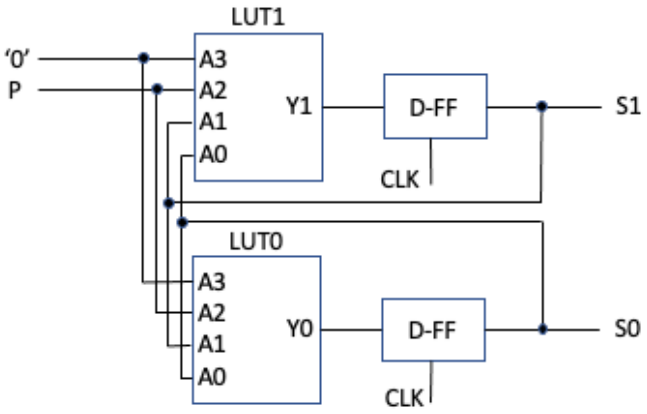

Figure 2.2

3. (a) *Figure 3.1* shows an R-2R ladder network. Derive from first principles and with clear justifications the values of I_0 to I_3 and V_0 to V_3 in terms of V_{REF} and R.

[5]

(b) *Figure 3.2* shows a ladder network which is NOT an R-2R structure. Derive from first principles and with clear justifications the values of I_0 to I_3 and V_0 to V_3 in terms of V_{REF} and R for this new ladder network.

[10]

(c) The ladder network in *Figure 3.2* is used to implement a 4-bit DAC as shown in *Figure 3.3*. Explain how this circuit works as a non-binary weighted DAC converter.

[5]

(d) Assuming V_{REF} is 5V, and the switch control values X3:X0 is 4'b1010 as shown, what is the voltage at the output of the op-amp?

[5]

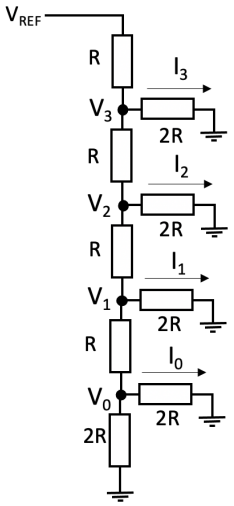

Figure 3.1

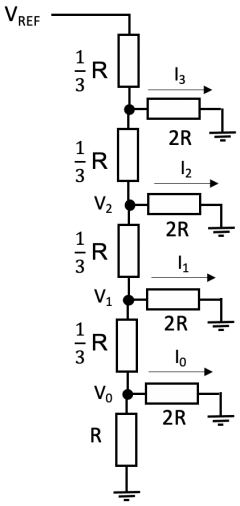

Figure 3.2

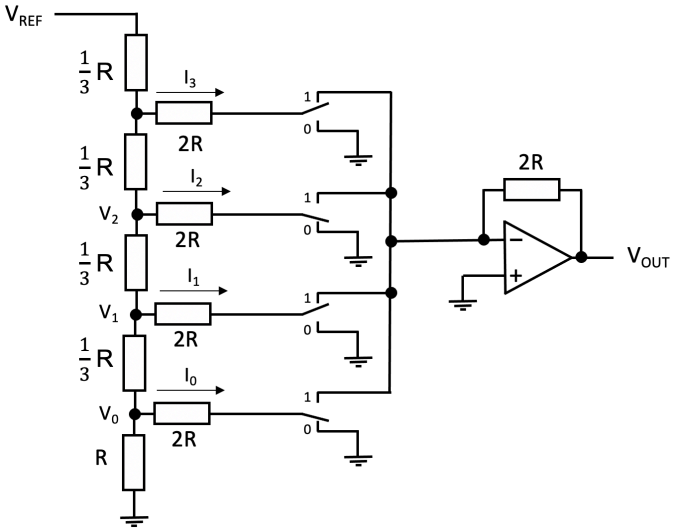

Figure 3.3

MCP601/1R/2/3/4

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Input Pins ..... ±2 mA
Analog Inputs (V_{IN}+, V_{IN}–) †† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current ..... Continuous
Current at Output and Supply Pins ..... ±30 mA
Storage Temperature ..... –65°C to +150°C
Maximum Junction Temperature (T_J) ..... +150°C
ESD Protection On All Pins (HBM; MM) ..... ≥ 3 kV; 200V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, and R_L = 100 kΩ to V_L, and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-2	±0.7	+2	mV	
Industrial Temperature	V_{OS}	-3	±1	+3	mV	T_A = -40°C to +85°C **(Note 1)**
Extended Temperature	V_{OS}	-4.5	±1	+4.5	mV	T_A = -40°C to +125°C **(Note 1)**
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±2.5	—	µV/°C	T_A = -40°C to +125°C
Power Supply Rejection	PSRR	80	88	—	dB	V_{DD} = 2.7V to 5.5V
Input Current and Impedance						
Input Bias Current	I_B	—	1	—	pA	
Industrial Temperature	I_B	—	20	60	pA	T_A = +85°C **(Note 1)**
Extended Temperature	I_B	—	450	5000	pA	T_A = +125°C **(Note 1)**
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common Mode						
Common Mode Input Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} – 1.2	V	
Common Mode Rejection Ratio	CMRR	75	90	—	dB	V_{DD} = 5.0V, V_{CM} = -0.3V to 3.8V
Open-loop Gain						
DC Open-loop Gain (large signal)	A_{OL}	100	115	—	dB	R_L = 25 kΩ to V_L, V_{OUT} = 0.1V to V_{DD} – 0.1V
	A_{OL}	95	110	—	dB	R_L = 5 kΩ to V_L, V_{OUT} = 0.1V to V_{DD} – 0.1V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 20	mV	R_L = 25 kΩ to V_L, Output overdrive = 0.5V
	V_{OL}, V_{OH}	V_{SS} + 45	—	V_{DD} – 60	mV	R_L = 5 kΩ to V_L, Output overdrive = 0.5V
Linear Output Voltage Swing	V_{OUT}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 25 kΩ to V_L, A_{OL} ≥ 100 dB
	V_{OUT}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 5 kΩ to V_L, A_{OL} ≥ 95 dB
Output Short Circuit Current	I_{SC}	—	±22	—	mA	V_{DD} = 5.5V
	I_{SC}	—	±12	—	mA	V_{DD} = 2.7V
Power Supply						
Supply Voltage	V_{DD}	2.7	—	6.0	V	**(Note 2)**
Quiescent Current per Amplifier	I_Q	—	230	325	µA	I_O = 0

Note 1: These specifications are not tested in either the SOT-23 or TSSOP packages with date codes older than YYWW = 0408. In these cases, the minimum and maximum values are by design and characterization only.

2: All parts with date codes November 2007 and later have been screened to ensure operation at V_{DD}=6.0V. However, the other minimum and maximum specifications are measured at 1.4V and/or 5.5V.

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, and R_L = 100 kΩ to V_L, C_L = 50 pF, and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Frequency Response						
Gain Bandwidth Product	GBWP	—	2.8	—	MHz	
Phase Margin	PM	—	50	—	°	G = +1 V/V
Step Response						
Slew Rate	SR	—	2.3	—	V/µs	G = +1 V/V
Settling Time (0.01%)	t_{settle}	—	4.5	—	µs	G = +1 V/V, 3.8V step
Noise						
Input Noise Voltage	E_{ni}	—	7	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	29	—	nV/√Hz	f = 1 kHz
	e_{ni}	—	21	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

MCP603 CHIP SELECT ($\overline{CS}$) CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.7V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, and R_L = 100 kΩ to V_L, C_L = 50 pF, and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	-1.0	—	—	µA	$\overline{CS}$ = 0.2V_{DD}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.7	2.0	µA	$\overline{CS}$ = V_{DD}
Shutdown V_{SS} current	I_{Q_SHDN}	-2.0	-0.7	—	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage in Shutdown	I_{O_SHDN}	—	1	—	nA	
Timing						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	3.1	10	µs	$\overline{CS}$ ≤ 0.2V_{DD}, G = +1 V/V
$\overline{CS}$ High to Amplifier Output High-Z Time	t_{OFF}	—	100	—	ns	$\overline{CS}$ ≥ 0.8V_{DD}, G = +1 V/V, No load.
Hysteresis	V_{HYST}	—	0.4	—	V	V_{DD} = 5.0V

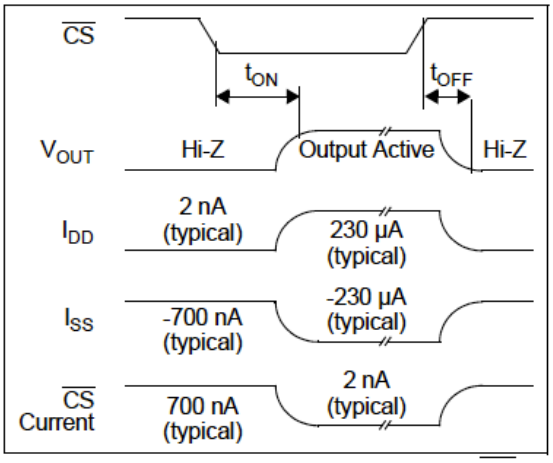

FIGURE 1-1: *MCP603 Chip Select ($\overline{CS}$) Timing Diagram.*

